MV601

REMOTE CONTROL RECEIVER

The MV601 is a remote control receiver designed to operate in conjunction with the MV500 transmitter. A five bit tristate binary output corresponding to the 32 codes available from the MV500 is provided together with data ready and output enable signals, allowing a simple interface to a microprocessor. A ceramic resonator and two rate inputs set the data rate to correspond to that produced by the MV500.

FEATURES

- High Noise Immunity
- 5V Operation
- Very Low Supply Current
- Momentary or Latched Operation
- Tri-State Outputs
- Ceramic Resonator and Data Rate Inputs to match MV500

APPLICATIONS

- Remote Control Interface to Microprocessor
- Industrial and Consumer Remote Control

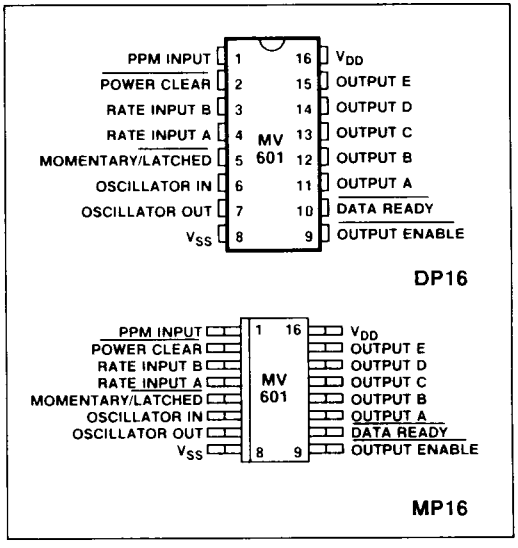


Fig 1 Pin connections - top view

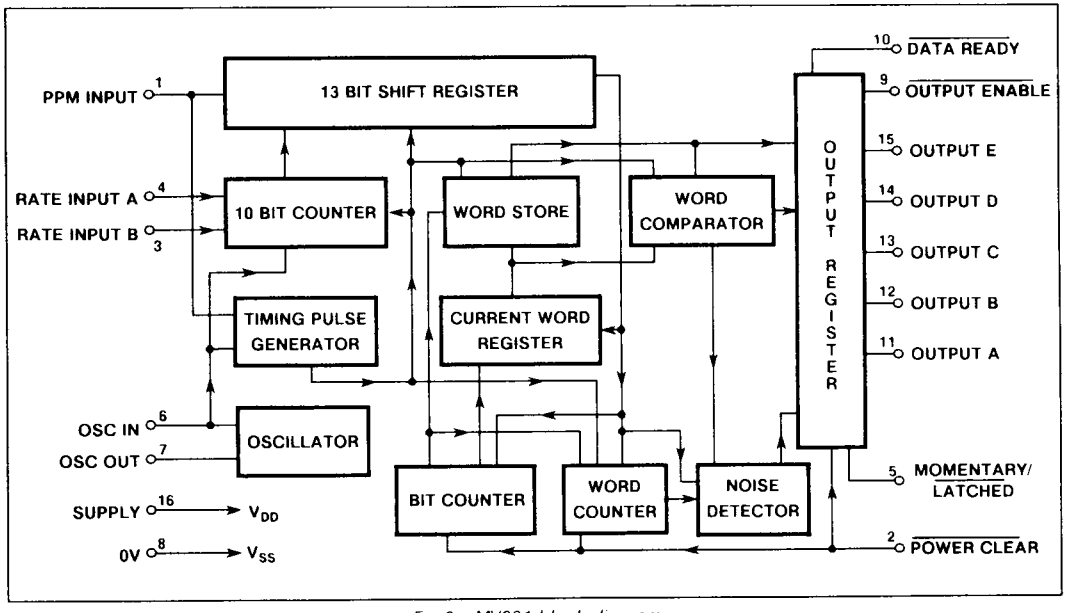


Fig.2 MV601 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0°C to 70°C, V_{DD} = +4.5V to +5.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Power supply current, I_{DD}	16		0.2	2.0	mA	
Oscillator frequency	6, 7			10	MHz	
INPUTS						
OSCIN, RATE A, RATE B,	6, 4, 3,					
MOM / $\overline{LAT}$, $\overline{OEN}$	5, 9					
Input low voltage (V_{IL})				V_{DD} / 3		
Input high voltage (V_{IH})		V_{DD} ×2/3				
PPM, $\overline{POWER\ CLEAR}$	1, 2					
Input low voltage (V_{IL})				1.0	V	V_{DD} = 5.0V
Input high voltage (V_{IH})		2.0			V	
Threshold voltage rising			1.85		V	
Threshold voltage falling			1.05		V	
$\overline{POWER\ CLEAR}$, RATE A, RATE B	2, 4, 3					
Input low current			-33	-100	μA	Nom. 150k pullup resistor
All other inputs except OSCIN Input current	1, 5, 9			±2.5	μA	V_{IN} = V_{SS} -0.3V to V_{DD} +0.3V
OSCIN	6					
Input current				±10	μA	V_{IN} = V_{SS} -0.3V to V_{DD} +0.3V
OUTPUTS						
A - E, $\overline{DATA\ READY}$						
Output low current (sink)		13	26		mA	V_{OL} = 0.4V
Output high current (source)		-21	-45		mA	V_{OH} = 2.4V
Output leakage current (A-E)				±10	μA	V_O V_{SS} -0.3 to V_{DD} + 0.3V pin 9 = V_{DD}
OSCOUT						
Output low voltage (sink)		1.0			mA	V_{IO} = 0.3V
Output high current (source)		-1.0			mA	V_{OH} = V_{DD} 0.3V

OPERATING NOTES

The MV601 is designed to operate in conjunction with the MV500 transmitter. When the rate inputs of MV500 and MV601 are programmed with the same binary input code and matched ceramic resonator frequencies are used (within 4%), the outputs of the MV601 will be set to the value of the PPM code transmitted. Two identical valid words must be received before an output response. A data ready signal, set after the output data has settled may be used to strobe data into an external register or generate an interrupt to a microprocessor.

When used in infra red systems, the PPM input will usually be derived from the output of an SL486 infra red amplifier, but direct connection to the transmitter is also possible. The PPM input is insensitive to pulse width.

The power clear input is generally connected to an external capacitor which holds the input momentarily low ensuring a reset of the outputs and internal logic at power on. The circuit can be reset at any time by taking the power clear input low.

The rate inputs have nominal 150kΩ pull up resistors and may therefore be left open circuit when a high input is required.

When more than 32 codes are required, the rate inputs on the MV500 transmitter can be switched and 2 or 3 MV601 circuits wired in parallel to the PPM signal. Only the MV601 with rate inputs identical to the transmitter will respond. An alternative method giving 64 possible codes from only one MV601 is shown in Fig. 7. The fastest and slowest rate settings from the transmitter should be used. In this circuit the three transistors produce a DC level dependent on the rate of the received PPM data. The DC level is used to provide the F output bit and to automatically switch the rate B input to the MV601 to correspond with the transmitter.

PIN FUNCTIONS

1. **PPM Input**
The serial PPM data is connected here. Pulse width is not critical but must remain high or low for at least one clock cycle.

2. **Power Clear**
A logic low resets the output register and internal logic ensuring full noise immunity from switch on. A capacitor to V_{SS} will normally be connected. A 150k (nom) resistor to V_{DD} is provided so that the input may be left open circuit if required.

3. **Rate Input B**
This input controls the received data rate according to table 1. Input state must match that on MV500. A 150k (nom) resistor pull up to V_{DD} is provided so that the input may be left open circuit if required.

4. **Rate Input A**
As pin 3.

5. **Momentary/Latched Input**
Controls the operational mode of the output register. When low, data will be retained at the output until updated by a newly validated code. When high, the data will only remain at the outputs whilst the valid code is present at the PPM input.

6. **Oscillator In**
The input to the oscillator circuit. A Pierce oscillator is formed by a ceramic resonator connected to pin 7 and capacitor connected to ground.

7. **Oscillator Out**
The output of the oscillator circuit. A capacitor connected to ground completes the Pierce oscillator circuit.

8. **V_{SS}**
The negative supply pin.

9. **Output Enable**
A logic low enables the A, B, C, D and E outputs. A logic high switches the output transistors off, providing a high impedance state.

10. **Data Ready**
Set low when valid data is present at the outputs.

11. **Output A**
Tri-state output set to the binary equivalent of the PPM input data.

12. **Output B**
As pin 11.

13. **Output C**
As pin 11.

14. **Output D**
As pin 11.

15. **Output E**
As pin 11.

16. **V_{DD}**
The positive supply pin.

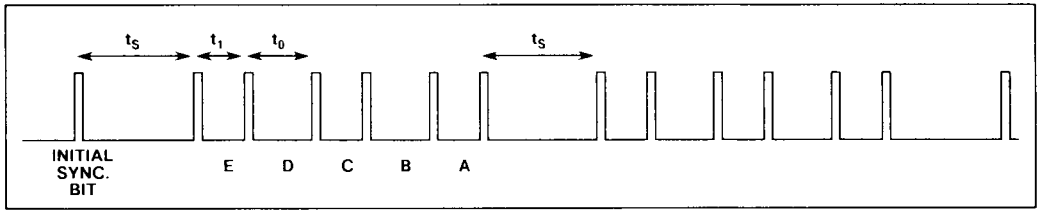


Fig.3 Typical Received PPM Data

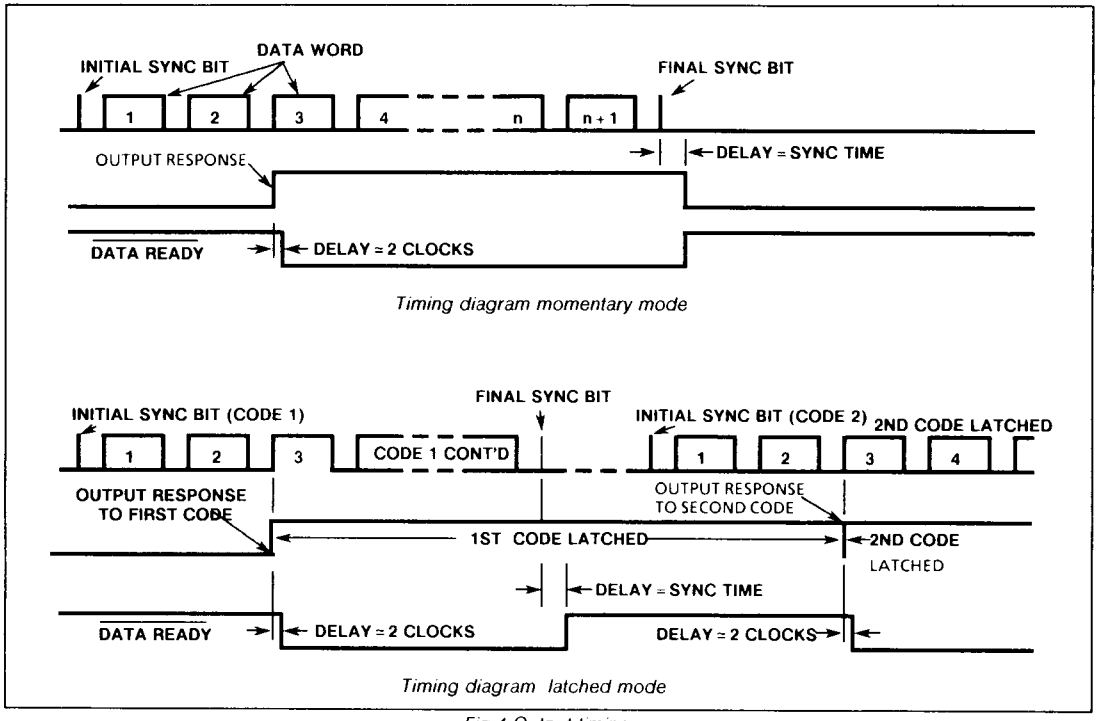
Rate inputs		Clock cycles		
B	A	t_1	t_0	t_S
0	0	NV	NV	NV
0	1	4096	6144	12288
1	0	2048	3072	6144
1	1	1024	1536	3072

Table 1 Rate control inputs

NV = Not Valid
NOTE: Rate inputs should match those on MV500

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD}	+7V
Input Voltage	V_{DD} + 0.3V to V_{SS}-0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +125°C
Output Sink and Source Current	50mA
Humidity	85%



Timing diagram momentary mode

Timing diagram latched mode

Fig.4 Output timing

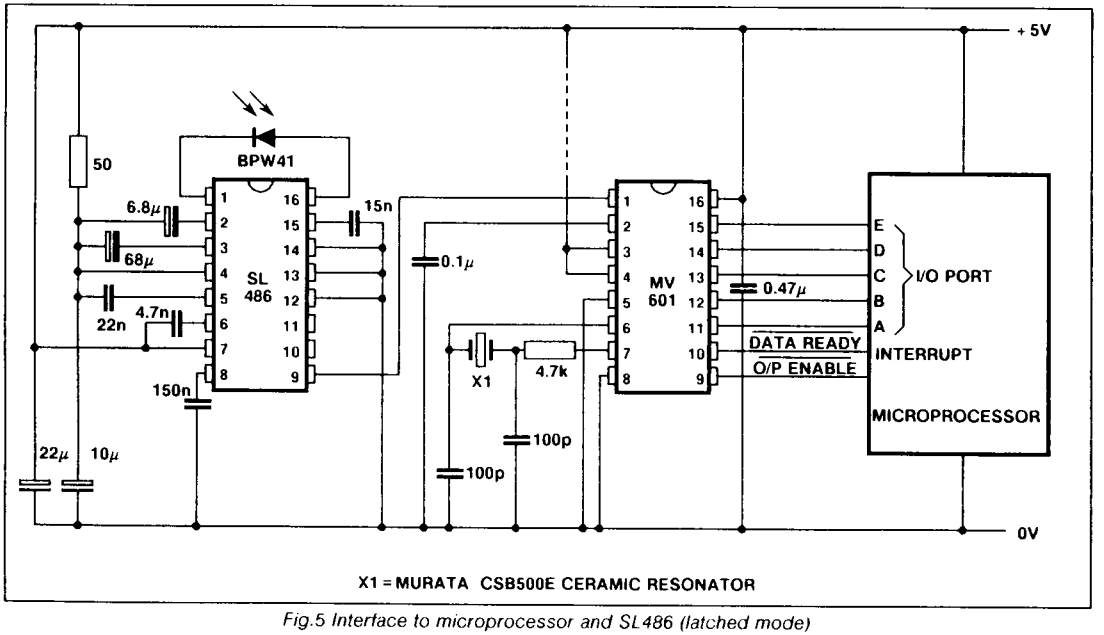


Fig.5 Interface to microprocessor and SL486 (latched mode)

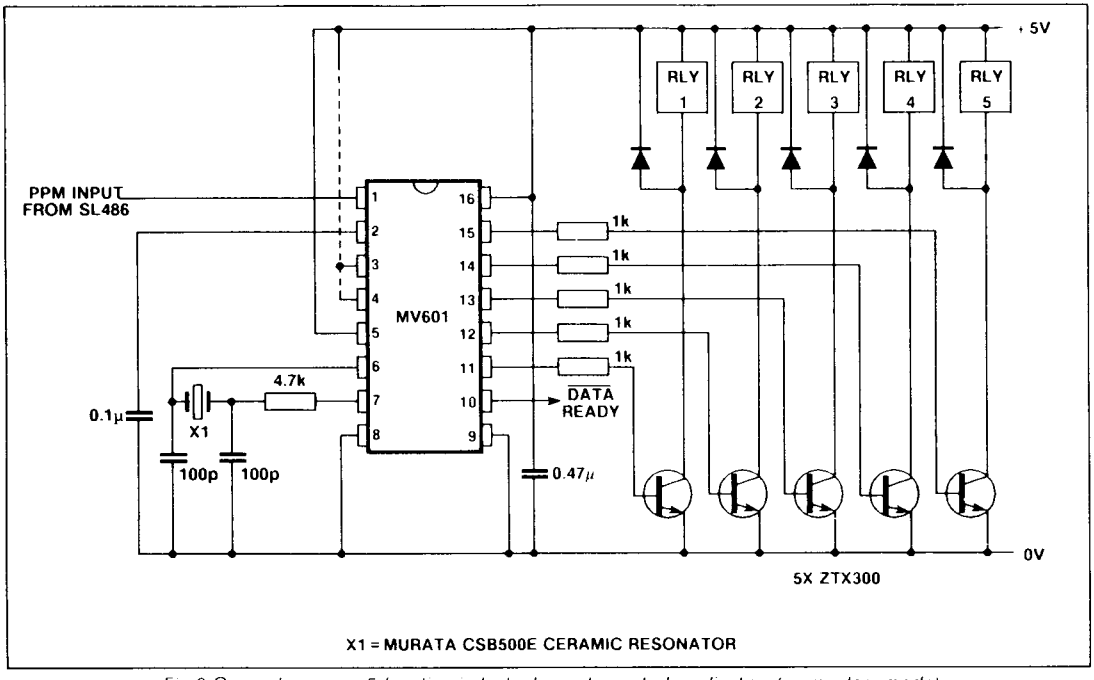


Fig.6 General purpose 5-function industrial remote control application (momentary mode)

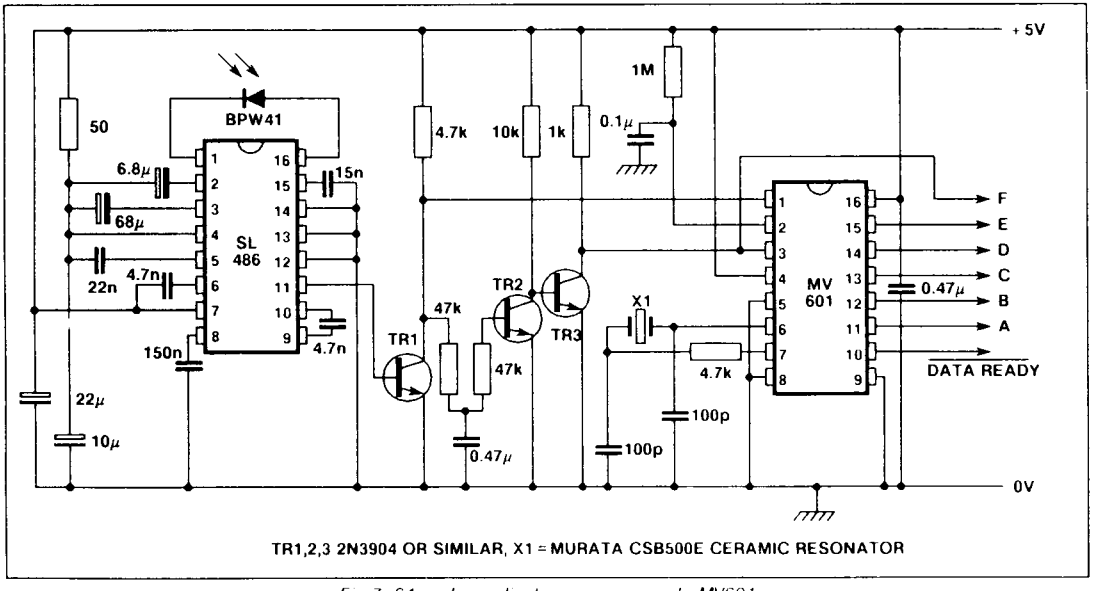


Fig.7 64-code application using a single MV601